Amendments to the Specification:

Please replace the paragraph beginning on page 2, line 32 through page 3, line 4 with the following rewritten paragraph:

In one aspect, an IF demodulator comprising: a first IF differentiator for differentiating an I signal; a second IF differentiator for differentiating a Q signal; a cross-coupled multiplier for multiplying the differentiated I signal with the ~~I~~ Q signal and multiplying the differentiated Q signal with the ~~Q~~ I signal to extract frequency information from the I signal and the Q signal; and a slicer for converting the frequency information to digital data is disclosed in the present invention.

Please replace the paragraph beginning on page 3, line 18 through page 4, line 6 with the following rewritten paragraph:

The objects, advantages and features of this invention will become more apparent from a consideration of the following detailed description and the drawings, in which:

FIG. 1 is an exemplary low-IF receiver architecture, according to one embodiment of the present invention;

FIG. 2 is an exemplary block diagram of an IF demodulator, according to one embodiment of the present invention;

FIG. 3 is an exemplary block diagram of an IF differentiator, according to one embodiment of the present invention;

FIG. 4 is an exemplary block diagram of ~~an~~ a slicer, according to one embodiment of the present invention;

FIG. 5 is an exemplary simplified circuit diagram of an IF differentiator, according to one embodiment of the present invention;

FIG. 6 is an exemplary simplified circuit diagram of a multiplier, according to one embodiment of the present invention;

FIG. 7 is an exemplary simplified circuit diagram of an offset tracker, according to one embodiment of the present invention; and

FIG. 8 is an exemplary simplified circuit diagram of a peak/valley detector, according to one embodiment of the present invention.

Please replace the paragraph beginning on page 6, line 22 through page 7, line 2 with the following rewritten paragraph:

A $\varphi(t)$, the analog signal at the input of the slicer 28 in FIG. 2, is applied to the inputs of the peak detector 41 and the valley detector 42 in FIG. 4. The peak detector 41 detects the ~~peack~~ peak of the analog input signal V_P and the valley detector 42 detect the valleys (minimums) of the analog input signal V_V. The offset tracking circuit 43 takes the average of V_P and V_V $((V_P + V_V)/2)$ to produce a DC average of the peak and valley. This DC average signal is compared with the original analog signal by comparator 44 to produce the desired digital output. At the output of comparator, a high signal is produced if the analog input signal is higher than its DC average value, and a low signal is produced if the analog input signal is lower than its DC average value. The Slow/Fast signal depicted in FIG. 4 indicates ~~wether~~ whether

the slicer must go to fast ~~attach~~ attack mode or slow decay mode described below.

Please replace the paragraph beginning on page 8, line 4 with the following rewritten paragraph:

FIG. 6 is an exemplary circuit implementation for multiplier ~~22~~ 25 (I multiplier) of FIG. 2. The Q multiplier 24 has a similar circuit implementation. The input stage of the multiplier (M3/M4) takes the differential input IN+ and IN- that is the output of the BPF 21 in FIG. 2. Transistors M5/M6 and M7/M8 form the differential pair Gilbert-type mixers that take the differential input LO+ and LO- to multiply LO signal by IN signal. As shown, the outputs of the I multiplier are connected to the outputs of the Q multiplier (not shown) to simply form the subtractor block 26 of FIG. 2. The common mode feedback (CMFB) 61 is used to adjust the DC output levels.

Please replace the paragraph beginning on page 9, line 21 with the following rewritten paragraph:

FIG. 8 is an exemplary simplified circuit diagram for a peak (or valley) detector (blocks 41 and 42 in FIG. 4). The peak/valley detectors take the ~~pick~~ peak (or valley) of the input signal as an input and charge the capacitor C to a peak (or a valley) using the OpAmp 81 and the PMOS transistor M80. However, since the leakage current of the capacitor C is small, the capacitor C takes a long time to charge or discharge in response to changes in peaks or valleys. OpAmp 81 is a differential pair OpAmp with single ended output.

When the signal at the input of the OpAmp increases, because of the OpAmp's high gain, its output goes to zero which in turn, turns transistor M80 on. That pulls the output voltage high to adjust the peak value.